**WHAT IS CLAIMED IS:**

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1. A data processing apparatus comprising:

a register file comprising a plurality of registers, each of said plurality of registers having a corresponding register number;

a first functional unit group connected to said register file and including a plurality of first functional units, said first functional unit group responsive to an instruction to

receive data from one of said plurality of registers corresponding to an instruction-specified first operand register number at a first operand input,

operate on said received data employing an instruction-specified one of said first functional units, and

output data to one of said plurality of registers corresponding to an instruction-specified first destination register number from a first output;

a second functional unit group connected to said register file and including a plurality of second functional units, said second functional unit group responsive to an instruction to

receive data from one of said plurality of registers corresponding to an instruction-specified second operand register number at a second operand input,

operate on said received data employing an instruction-specified one of said second functional units, and

output data to one of said plurality of registers corresponding to an instruction-specified second destination register number from a second output;

a first comparator receiving an indication of said first operand register number of a current instruction and an indication of said second destination register number of an

immediately preceding instruction, said first comparator indicating whether said first operand register number of said current instruction matches said second destination register number of said immediately preceding instruction; and

a first register file bypass multiplexer connected to said register file, said first functional unit group, said second functional unit group and said first comparator having a first input receiving data from said register corresponding to said first operand register number of said current instruction, a second input connected to said second output of said second functional unit group and an output supplying an operand to said first operand input of said first functional unit group, said first multiplexer selecting said data from said register corresponding to said first operand number of said current instruction if said first comparator fails to indicate a match and selecting said second output of said second functional unit group if said first comparator indicates a match.

2. The data processing apparatus of claim 1, wherein said register file, said first functional unit group, said second functional unit group, said first comparator and said first register file bypass multiplexer operate according to an instruction pipeline comprising:

a first pipeline stage consisting of a register read operation from said register file and a first half of operation of a selected functional unit of said first and said second functional unit groups, and

a second pipeline stage consisting of a second half of operation of said selected functional unit of said first and said second functional unit groups and a register write operation to said register file,

wherein the sum of the time of said register read operation and said register write operation equals approximately the sum of

the time of said first and second halves of operation of a slowest of said functional units of said first and second functional unit groups.

3. The data processing apparatus of claim 1, further comprising an output register having an input connected to said second output of said second functional unit group and an output connected to said register file for temporarily storing said output of said second functional unit group prior to storing in said register corresponding to said second destination register number,

wherein said first comparator further receives an indication of said second destination register number of a second preceding instruction, said first comparator further indicating whether said first operand register number of said current instruction matches said second destination register number of said second preceding instruction, and

wherein said multiplexer further has a third input connected to said output register output, said multiplexer selecting said output register output if said first comparator indicates a match.

4. The data processing apparatus of claim 3, wherein said register file, said first functional unit group, said second functional unit group, said first comparator, said first register file bypass multiplexer, and said output register operate according to an instruction pipeline comprising:

a first pipeline stage consisting of a register read operation from said register file;

a second pipeline stage consisting of an operation of a selected functional unit of said first and second functional unit groups; and

a third pipeline stage consisting of a register write operation to said register file,

wherein the time of said register read operation and the time of said register write operation are each equal approximately to the time of operation of a slowest of said selected functional units of said first and second functional unit groups.

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5. The data processing apparatus of claim 1, said first comparator further receiving an indication of said first destination register of said immediately preceding instruction, said first comparator further indicating whether said first operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said first multiplexer further having a third input connected to said first output of said first functional unit group, and said first multiplexer selecting said first output of said first functional unit group if said first comparator indicates a match.

6. The data processing apparatus of claim 1, said first functional unit group further responsive to an instruction to receive data from one of said plurality of registers corresponding to an instruction-specified third operand register number at a third operand input,

said apparatus further comprising:

a second comparator receiving an indication of said third operand register number of a current instruction and an indication of said second destination register number of said immediately preceding instruction, said second comparator indicating whether said third operand register number of said current instruction matches said second destination register number of said immediately preceding instruction; and

a second register file bypass multiplexer connected to said register file, said first functional unit group, said second functional unit group and said second comparator having a first input receiving data from said register corresponding to said third operand register number of said current instruction, a second input connected to said second output of said second functional unit group and an output supplying an operand to said third operand input of said first functional unit group, said second multiplexer selecting said data from said register corresponding to said third operand number of said current instruction if said second comparator fails to indicate a match and selecting said second output of said second functional unit group if said second comparator indicates a match.

7. The data processing apparatus of claim 6, said first comparator further receiving an indication of said first destination register of said immediately preceding instruction, said first comparator further indicating whether said first operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said first multiplexer further having a third input connected to said first output of said first functional unit group, said first multiplexer selecting said first output of said first functional unit group if said first comparator indicates a match,

said second comparator further receiving an indication of said first destination register of said immediately preceding instruction, said second comparator further indicating whether said third operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said second multiplexer further having a third input connected to said first output of said first functional unit group, and said second multiplexer

selecting said first output of said first functional unit group if said second comparator indicates a match.

8. The data processing apparatus of claim 1 further comprising:

a third comparator receiving an indication of said second operand register number of a current instruction and an indication of said second destination register number of an immediately preceding instruction, said third comparator indicating whether said second operand register number of said current instruction matches said second destination register number of said immediately preceding instruction; and

a third register file bypass multiplexer connected to said register file, said first functional unit group, said second functional unit group and said third comparator having a first input receiving data from said register corresponding to said second operand register number of said current instruction, a second input connected to said second output of said second functional unit group and an output supplying an operand to said second operand input of said second functional unit group, said third multiplexer selecting said data from said register corresponding to said second operand number of said current instruction if said third comparator fails to indicate a match and selecting said second output of said second functional unit group if said third comparator indicates a match.

9. The data processing apparatus of claim 8, said third comparator further receiving an indication of said first destination register number of an immediately preceding instruction, said third comparator indicating whether said second operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said third multiplexer further having a third input

connected to said first output of said first functional unit group, and said third multiplexer further selecting said first output of said first functional unit group if said third comparator indicates a match.

10. The data processing apparatus of claim 1 further comprising a third functional unit group connected to said register file, wherein said third functional unit group's register file output data is available for register file bypass solely within the third functional unit group itself.

11. A data processing apparatus comprising:

a first register file comprising a plurality of registers, each of said plurality of registers having a corresponding register number;

a second register file comprising a plurality of registers, each of said plurality of registers having a corresponding register number;

a first functional unit group including an input connected to said first and second register files, an output connected to said first register file, and a plurality of first functional units, said first functional unit group responsive to an instruction to

receive data from one of said plurality of registers in said first and second register files corresponding to an instruction-specified first operand register number at a first operand input,

operate on said received data employing an instruction-specified one of said first functional units, and

output data to one of said plurality of registers in said first register file corresponding to an instruction-specified first destination register number from a first output;

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a second functional unit group including an input connected to said first and second register files, an output connected to said second register file, and a plurality of second functional units, said second functional unit group responsive to an instruction to

receive data from one of said plurality of registers in said first and second register files corresponding to an instruction-specified second operand register number at a second operand input,

operate on said received data employing an instruction-specified one of said second functional units, and

output data to one of said plurality of registers in said second register file corresponding to an instruction-specified second destination register number from a second output; and

a first crosspath connecting said second register file to said first functional unit group comprising

a first crosspath comparator, wherein, if said first operand register is in said second register file, said comparator receives an indication of said first operand register number of a current instruction and an indication of said second destination register number of a preceding instruction, and said first crosspath comparator indicates whether said first operand register number of said current instruction matches said second destination register number of said preceding instruction, and

a first crosspath multiplexer connected to said second register file, said first functional unit group, said second functional unit group and said first crosspath comparator having a first input receiving data from said register corresponding to said first operand register number of said current instruction, a second input connected to said second output of said second functional unit group and an output

supplying an operand to said first operand input of said first functional unit group, wherein, if said first operand register is in said second register file, said first crosspath multiplexer selects said data from said register corresponding to said first operand number of said current instruction if said first crosspath comparator fails to indicate a match and selects said second output of said second functional unit group if said first crosspath comparator indicates a match.

12. The data processing apparatus of claim 11 further comprising a second crosspath connecting said first register file to said second functional unit group.

13. The data processing apparatus of claim 11, said first crosspath further comprising a first crosspath register latching said crosspath multiplexer's output for said first functional unit group's first operand input.

14. The data processing apparatus of claim 11 further comprising a third functional unit group including an input connected to said first and second register files, an output connected to said first register file, and a plurality of third functional units, said third functional unit group responsive to an instruction to

receive data from one of said plurality of registers in said first and second register files corresponding to said instruction-specified first operand register number at a third operand input,

operate on said received data employing an instruction-specified one of said third functional units, and

output data to one of said plurality of registers in said first register file corresponding to an instruction-specified third destination register number from a third output,

said first crosspath further connecting said second register file to said third functional unit group, and said first crosspath multiplexer further having an output supplying an operand to said third operand input of said third functional unit group.

15. The data processing apparatus of claim 11 further comprising:

a first input comparator receiving an indication of said first operand register number of a current instruction, said first comparator indicating whether said first operand register number is in said first register file or said second register file; and

a first input multiplexer having a first input connected to said first register file, a second input connected to said first crosspath, and an output connected to said first functional unit group, said first input multiplexer selecting said first input if said first input comparator indicates said register corresponding to said first operand number is in said first register file, and selecting said second input if said first input comparator indicates said register corresponding to said first operand number is in said second register file.

16. The data processing apparatus of claim 15 further comprising a fourth functional unit group including an input connected to said first and second register files, an output connected to said first register file, and a plurality of fourth functional units, said fourth functional unit group responsive to an instruction to

receive data from one of said plurality of registers in said first or second register files corresponding to an instruction-specified fourth operand register number at a fourth operand input,

operate on said received data employing an instruction-specified one of said fourth functional units, and

output data to one of said plurality of registers in said first register file corresponding to an instruction-specified fourth destination register number from a fourth output,

said first input comparator further receiving an indication of said fourth destination register number of an immediately preceding instruction, said input first comparator indicating whether said first operand register number of said current instruction matches said fourth destination register number of said immediately preceding instruction, and

said first input multiplexer further having a third input connected to said fourth output of fourth functional unit group, said first multiplexer selecting said fourth output of said fourth functional unit group if said first input comparator indicates a match.

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